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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 10992304-3

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on May 23, 2006

Signature: /Edouard Garcia/

Typed or printed name: Edouard Garcia

Application Number	Filed
10/692,884	Oct. 24, 2003

First Named Inventor: Alfred I-Tsung Pan

Art Unit	Examiner
2822	Guerrero, Maria F.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [ ] attorney or agent of record. Registration number _____.
- [x] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34: 38,461

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Telephone number

May 23, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [x] *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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OIPE IAP64 MAY 26 2006 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Alfred I-Tsung Pan
Serial No. : 10/692,884
Filed : October 24, 2003
Title : MONOLITHIC COMMON CARRIER

Art Unit : 2822
Examiner : Guerrero, Maria F.

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

I. Status of Claims

Claims 14-36 are pending.

Claims 22-36 have been allowed.

Claims 14-21 have been rejected and are the subject of this Pre-Appeal Brief Request for Review.

II. Claim Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 14-18, 20, and 21 under 35 U.S.C. § 102(b) over Wilson (U.S. 4,890,157).

A. Independent Claim 14

As explained in detail below, the Examiner's rejection of independent claim 1 should be withdrawn because Wilson does not teach "adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision," nor does Wilson teach "lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances."

CERTIFICATE OF MAILING

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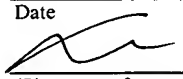

(Signature of person mailing papers)

Edouard Garcia
(Typed or printed name of person mailing papers)

1. Wilson's disclosure

Wilson discloses an integrated circuit product that includes IC chips 30 mounted on a multilayer polyimide and conductor film 17 (referred to herein as the "film assembly 17").

Wilson teaches that a casting process is used to form the film assembly 17 on, e.g., a polished, oxidized, circular silicon or quartz substrate 10 (see 2: 35-56 and 5:14-40).[1] After the film assembly 17 has been formed, it is cured (see 2:57-61 and 5:41-45). Next, chip connection pads are created on the cured film assembly 17 (see 5:46-50). The IC chips 30 are soldered to the connection pads (see 2:61-62 and 6:3-13).

A template 40 is used to facilitate the alignment and attachment of the IC chips 30 to the film assembly 17 (see 6:38 - 7:33). In this regard, the film assembly 17 is clamped between the template 40 and a backing plate 41 using alignment pins 43-45 and spring loaded nuts 51-53 (see 6:65 - 7:7). Next, the IC chips 30 are placed in the appropriate holes 58 in the template 40 (see 7:8-12) and the entire assembly is heated to solder the IC chips 30 to the film assembly 17 (see 7:29-33).

The film assembly 17 and the soldered IC ships 30 then are removed from the substrate 10 using a swelling agent (see 2:62-65 and 6:14-34). After removal from the substrate 10, the film assembly 17 can be cut for packaging (see 6:35-37 and 7:54-56) and bonded to a motherboard or lead frame (see the Abstract, 3:5-10, and 7:54- 8:26).

2. The Examiner's position and Applicant's rebuttal

i. The Examiner's first position

The Examiner has taken the position that Wilson discloses "adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision" in col. 7, lines 34-54 (see ¶ 4 of the final Office action).

Contrary to the Examiner's first position, Wilson does not adhere unprocessed integrateable forms of a plurality of chips on the upper surface of a carrier substrate. Instead, the integrated circuit chips 30 that are affixed to the upper surface of a multilayer film 17 in accordance with Wilson's teachings are completely processed into integrated circuit chips before they are affixed to the multilayer film 17 (see, e.g., 2:57-65).

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[1] In this Request, citations to parts of Wilson's disclosure are formatted as col:line. For example, 2:35-56 refers to column 2, lines 35-56 of Wilson's disclosure.

The specification of the pending application defines "an unprocessed, integratable chip" as "a workpiece of material which can be lithographically processed to form an integrated device or chip, and which has not yet been exposed to lithographic processing steps" (page 5, lines 20-23). One skilled in the art at the time the invention was made would have understood from Wilson's disclosure that the IC chips 30 are completed integrated circuit chips that are ready to be soldered to the conductors on the film assembly 17 (see, e.g., 7:7-12). In accordance with the ordinary and accustomed practice in the art at the time the invention was made, such completed IC chips 30 would have been exposed to lithographic processing steps and therefore would not correspond to "unprocessed, integratable chips" in accordance with the definition provided in the specification. Wilson does not teach anything that is inconsistent with this ordinary an accustomed practice in the art.

In the section of Wilson's disclosure cited in support of the Examiner's position (i.e., 7:34-54), Wilson merely teaches that photolithographic techniques are used to place patterns on the film assembly 17 for defining the pin alignment holes 54-56 (see FIG. 3) and to place patterns on the template 40 for defining the pin alignment holes 47-49 and the IC chip alignment holes 58 (see FIG. 3). This disclosure does not teach anything about the nature of the IC chips 30, either before or after they are soldered to the film assembly 17.

ii. The Examiner's second position

The Examiner also has taken the position that Wilson discloses "lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances" in the Abstract, 2:35-68, and 7:34-54 (see ¶ 4 of the final Office action).

After the IC chips 30 have been soldered to the film assembly 17, however, Wilson does not lithographically process the IC chips 30 to form a plurality of integrated chips on the upper surface of the film assembly 17. Indeed, as explained above, the integrated circuit chips 30 already are "formed" into integrated circuit chips before they are soldered to the film assembly 17.

In the section of Wilson's disclosure cited in support of the Examiner's second position (i.e., the Abstract, col. 2, lines 35-68, and col. 7, lines 34-54), Wilson teaches in pertinent part that after the IC chips 30 have been soldered to the film assembly 17, the completed integrated circuit product (i.e., the film assembly 17 and the soldered IC chips 30;

referred to as a "chip-film structure 74" and a "daughter film 90" in 7:54 - 8:26 of Wilson) may be bonded to a mother board or leadframe. In accordance with the ordinary and accustomed practice in the art at the time the invention was made, such processing does not involve lithographically processing the IC chips 30 to form a plurality of integrated chips on the upper surface of the film assembly 17. Instead, such processing typically involves mounting the completed integrated circuit product to the motherboard or leadframe and bonding conductors on the film assembly 17 to the conductors on the motherboard or leadframe (see, e.g., 7:54 - 8:26 and FIGS. 4 and 5 of Wilson).

It is noted that the Examiner's citation to the photolithographic techniques described in 7:34-54 of Wilson in support of her second position is misplaced because these photolithographic techniques are not applied to the IC chips 30. Instead, these photolithographic techniques are performed on the film assembly 17 and the template 40. In addition, these photolithographic techniques are performed before the IC chips 30 are aligned with and soldered to the film assembly 17.

For at least these reasons, the Examiner's rejection of independent claim 14 under 35 U.S.C. § 102(b) over Wilson should be withdrawn.

B. Claims 15-18, 20, and 21

Each of claims 15-18, 20, and 21 incorporates the features of independent claim 14 and therefore is patentable over Wilson for at least the same reasons explained above.

III. Claim Rejections under 35 U.S.C. § 103

The Examiner has rejected claim 19 under 35 U.S.C. § 103(a) over Wilson in view of Leibovitz (U.S. 5,055,425).

Claim 19 incorporates the features of independent claim 14. Leibovitz does not make-up for the failure of Wilson to teach or suggest the features recited in claim 14. Indeed, the Examiner has cited Leivovitz only for his disclosure of "using polishing to remove surface irregularities and prepare the surface for the subsequent processing" (see ¶ 5 of the final Office action). Therefore, claim 19 is patentable over Wilson and Leibovitz for at least the same reasons explained above in connection with claim 14.

IV. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 08-2025.

Respectfully submitted,

Date: May 23, 2006

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